BROADBAND HIGH-EFFICIENCY HBT MMIC POWER AMPLIFIER FABRICATED WITH RE-ALIGNED PROCESS

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ABSTRACT

The design and performance of a 6 to 10 GHz Heterojunction Bipolar Transistor MMIC power amplifier that produces 1.25 to 2.15 Watts at 30 to 46 % power-added efficiency with 9.5 to 12.5 dB of power gain will be described. With only 500 μm^2 of output periphery, record MMIC HPA power densities of 2.5 to 4.3 $mW/\mu m^2$ have been demonstrated.

HBT DEVICE

The amplifier reported in this work was fabricated using a contact lithography based re-aligned AlGaAs/GaAs power HBT process. The epitaxial layers were grown using Low Pressure Organo-Metallic Vapor Phase Epitaxy (LPOMVPE), with Carbon as the base layer dopant for reliable operation under high current bias. The HBT structures were: n^+ cap $In_xGa_{1-x}As$ graded from x = 0 to 50% at the surface ($1x10^{19}$ cm^{-3} 35 nm), n^+ GaAs ($4x10^{18}$ cm^{-3} 170 nm), n $Al_xGa_{1-x}As$ ($5x10^{17}$ cm^{-3} 210 nm graded from x = 25% to 0 at both ends), p^+ GaAs base ($2x10^{19}$ cm^{-3} 70 nm), n^- GaAs collector ($5x10^{15}$ cm^{-3} 790 nm), and n^+ GaAs subcollector ($4x10^{18}$ cm^{-3} 450 nm) grown on 2° off (100)-oriented GaAs semi-insulating substrates. Si was used as the dopant in the n layers, and no spacer layer is needed between the GaAs base and AlGaAs emitter layers.

The device cell layout was optimized considering yield, thermal, and electrical constraints simultaneously. The base ohmic contacts were optically re-aligned to the emitter strips. The spacing between the two is kept around 1 μm. The resultant sub-cell geometry is 2 emitter fingers of 1.25 μm by 10 μm dimensions, with five sub-cells at 37.5 μm center-to-center separation per 125 μm^2 cell as shown in Figure 1. Discrete test devices utilized for characterization were thinned to 1 mil (25 μm), attached to Au-plated Brass carriers with Indium Lead solder. Laboratory power measurements of device performance at 9 GHz is summarized in Figure 2. The data given is for the common emitter configuration in class AB_2, class B, and class C operation with V_{ce} = 6 Volts.

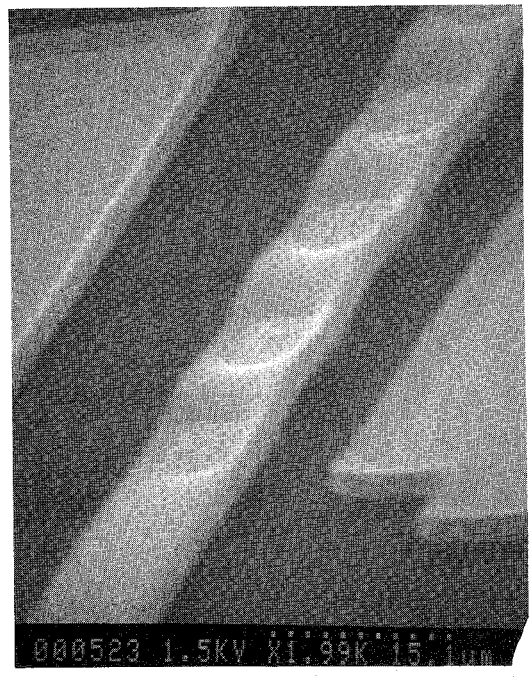


Figure 1: HBT Device Cell (125 μm^2, 2 Emitter Fingers per Sub-cell, Five Sub-cells)

Power(mW)	PAE(%)	Gain(dB)	Power Density($mW/\mu m^2$)
512	57	7.2	4.1
412	61	7.3	3.3
350	62	5.9	2.8

Figure 2: HBT Device Cell Performance (9 GHz, common emitter, with V_{ce} = 6 Volts, class AB_2, class B, class C)

CIRCUIT DESIGN

The design of this power amplifier is based upon a comprehensive methodology that includes both measurements and linear/non-linear modeling. De-embedded small signal S-parameters of the device were measured and the equivalent circuit model shown in Figure 3 was fitted to the data. Small signal models were created at both V_{ce} = 3 Volts and V_{ce} = 6 Volts with a collector current of I_c = 5 mA,

corresponding to the quiescent class AB_2 operating condition of the two devices in the cascode connection. Measurement of I/V characteristics, augmented with optimum load/contour data obtained via load pull were used to derive a consistent non-linear model, as well as a parallel RC equivalent of the optimum load impedance. The measured load-pull data and both the linear and non-linear models are then employed in the analysis and optimization of the design.

The amplifier, shown schematically in Figure 4, based upon improvements to the design described in [3], consists of a cascode (common emitter-common base) connection of the individual 125 μm^2 HBT cells to form a compound transistor, yielding the gain of a two-stage design in the area occupied by a single-stage amplifier. The common emitter stage provides the voltage gain, while the common base stage provides the current gain. Furthermore, the common emitter stage is operated at a low V_{ce}, increasing F_t and thus gain, while the common base stage operates at a high V_{ce}, maximizing power output and efficiency. Four 125 μm^2 cells of each configuration (CE/CB) are employed with classic Chebyshev low-pass structures used for impedance transformation. The design, unlike that in [3], incorporates integral bias networks on chip (DC blocking capacitors and base bias current provided with collector to base feedback resistors), and requires a single supply for operation.

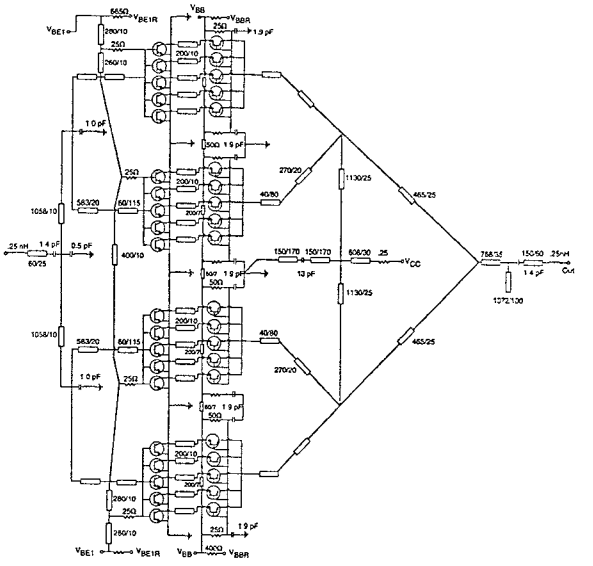
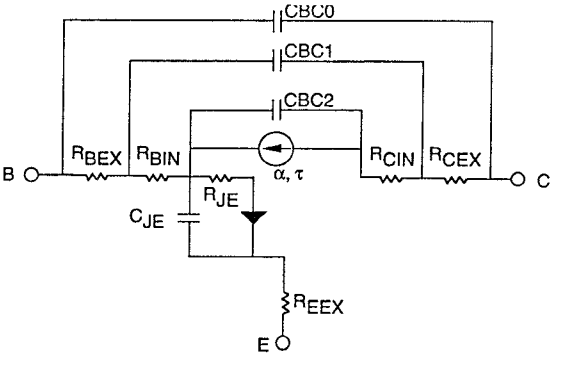


Figure 4: Simplified Schematic of HBT MMIC HPA (Dimensions are length/width in μm)



V_{CE} = 6 Volts I_{CE} = 5 mA

R_{BEX}	= 6.35 Ω	R_{EEX}	= 19.2 Ω
R_{BIN}	= 2.6 Ω	C_{JE}	= 4.98 pF
R_{JE}	= 1.37 Ω	CBC0	= .006 pF
R_{CIN}	= 6.79 Ω	CBC1	= .012 pF
R_{CEX}	= .67 Ω	CBC2	= .011 pF
α	= .931	A_E	= 25 μm^2
τ	= .16 pSEC		

Figure 3: Small-signal HBT Device Cell Model at Quiescent Bias Point

A significant portion of the design effort was devoted to thermal design of the MMIC. Finite-Element Analysis (FEA) was employed to calculate junction temperatures when the MMIC was solder attached to a Au-plated molybdenum carrier whose base is held at a constant temperature. Parameters used in the analysis include emitter width, emitter length, number of emitters per sub-cell, emitter spacing, GaAs thickness, GaAs temperature-dependent material properties, and dissipated heat. As a result, the device cell topology described earlier was selected from the parametric variations analyzed, and the MMIC was thinned to 2 mils (50 μm). Figure 5 shows the maximum hot spot junction temperature versus time for a 500 μsec pulse width at a 50% duty cycle with the baseplate at 40°C after reaching thermal equilibrium. The physical location of the time slice corresponds to the central common-base sub-cell. Note that this HBT MMIC design runs higher junction temperatures than MESFET or HEMT MMIC's of comparable power output during initial portions of the pulse, but steady state has essentially been reached at mid-pulse. The analysis indicates that when thermal design is included as a prerequisite, junction temperatures of HBT amplifiers can be acceptably controlled enabling CW operation.

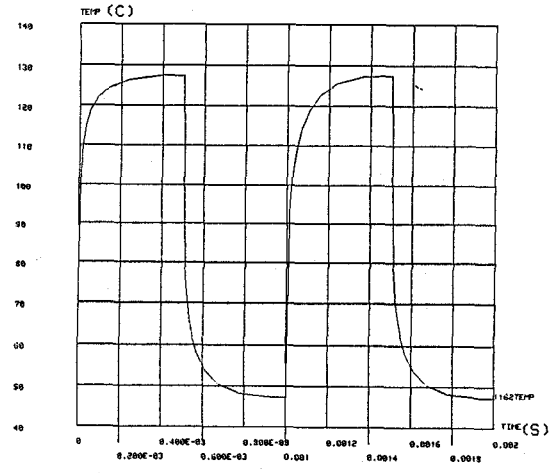


Figure 5: Maximum Junction Temperature vs Time for a 500 µsec Pulse Width at 50% Duty Cycle After Reaching Thermal Equilibrium

MMIC FABRICATION

Front side processing requires 13 mask levels, with two additional masks required for the backside. Device isolation is achieved with a combination of wet etch and ion implantation using Ar^+ and He^+. The emitter ohmic metal, after deposit and lift-off, is used as the etching mask for Reactive Ion Etching (RIE) of the emitter mesa. The base ohmic was defined and aligned to the emitter using contact optical lithography. Plasma Enhanced Chemical Vapor Deposition (PECVD) was employed to passivate the device with Silicon Nitride. The collector ohmic contact was opened through a sequence of dielectric and GaAs etch using dry techniques. Ohmic metal making contact with the n^+ subcollector is then alloyed. The additional MMIC steps of overlay metal, TaN thin film resistors, MIM capacitors, and air bridge metal complete the front side process. Via holes are fabricated by an anisotropic dry etch after lapping to a 2 mil thickness.

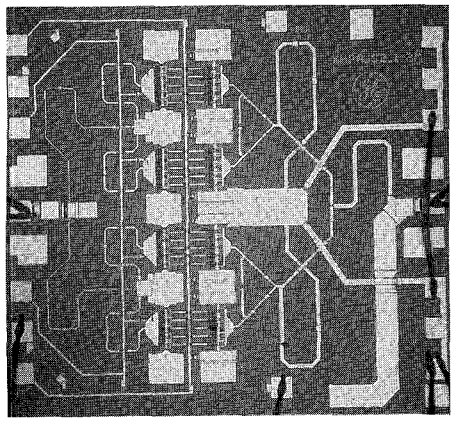


Figure 6: Broadband High-Efficiency HBT MMIC HPA (Chip size is 2.05 mm x 1.88 mm)

MEASURED RESULTS

The amplifiers, one of which is shown in Figure 6, were tested under both pulse and CW conditions after die attach to a Au-plated molybdenum carrier using Indium Lead solder. As shown in Figures 7 through 9, the amplifier produces 1.25 to 1.8 Watts at 30 to 46% power-added efficiency with 9.5 to 12.5 dB of power gain, under conditions of 100 µsec pulse width, 10% duty cycle with V_{cc} = 9 Volts. With higher supply voltage (V_{cc} = 10 Volts), the power improves 0.6 to 0.9 dB across frequency to 1.4 to 2.15 Watts with a 1% degradation in efficiency. At CW, power degrades by less than 0.2 dB, while gain degrades by less than 0.5 dB, a not unexpected result from the thermal analysis. With 500 μm^2 of output periphery, MMIC HPA power densities of 2.5 to 4.3 $mW/\mu m^2$ have been demonstrated. Figure 10 compares these results to those published in the references.

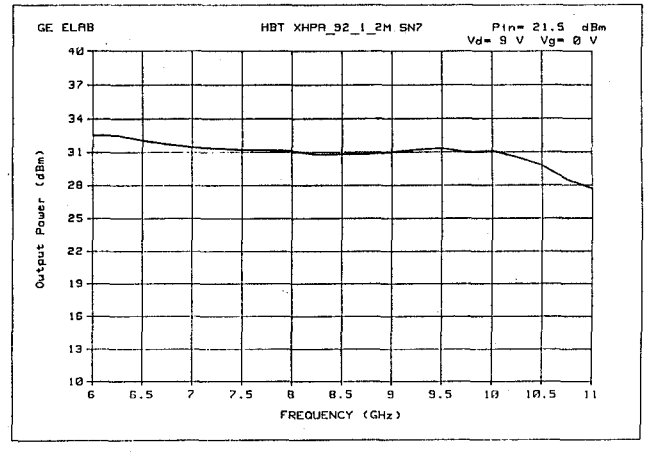


Figure 7: Power Output vs Frequency

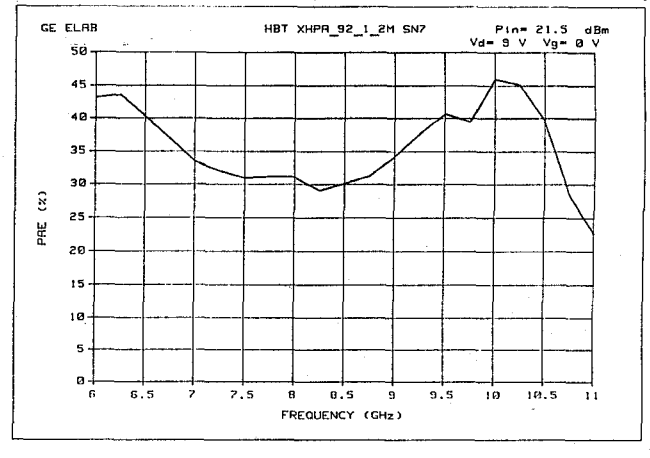


Figure 8: Power-Added Efficiency vs Frequency

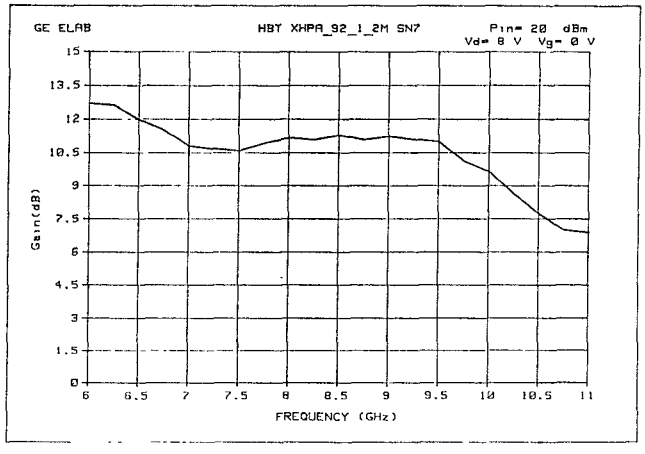


Figure 9: Power Gain vs Frequency

Reference	BW(GHz)	Gain(dB)	PAE(%)	P_D(mW/μm²)
[1]-4W	5	3-6	15-32	1.1-1.4
[1]-1W	5	6-9.5	23-39	0.9-1.4
[2]	0.8	8.5-10.5	25-36	1.1-1.7
[3]	3.5	11-13	26-47	1.2-1.9
This Work	4	9.5-12.5	30-46	2.5-4.3

Figure 10: Comparison of Reported X-Band HBT MMIC Amplifiers

ACKNOWLEDGEMENTS

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